IN THE CLAIMS:

1. (currently amended) A method of forming a field effect transistor comprising the steps of:

providing a semiconductor wafer of a ~~first semiconductor material~~ silicon having a device layer with a device layer lattice constant;

forming an epitaxial layer of a second semiconductor material on said device layer of said semiconductor wafer, said second material having a second lattice constant greater than said device lattice constant in a direction perpendicular to said wafer and said device layer lattice constant in a channel direction parallel to said wafer;

patterning said epitaxial layer of said second material to form at least one vertical side in said channel direction;

growing an epitaxial semiconductor channel layer of ~~said first semiconductor material~~ silicon on said vertical side, said channel layer having said second lattice constant perpendicular to said wafer and said device lattice constant along said channel direction, whereby said channel layer has tensile strain perpendicular to said channel direction and to said wafer;

forming a gate insulator in a body area of at least one vertical side of said channel;

forming a gate electrode abutting said gate insulator; and

forming source and drain electrodes in contact with opposite ends of said body area.

2. (currently amended) A method according to claim 1, in which ~~said first semiconductor material is silicon and~~ said second semiconductor material is SiGe.

3. (original) A method according to claim 1, in which said step of patterning said epitaxial layer comprises forming an island having two vertical sides separated by a transverse distance;

said step of forming said channel layer forms said channel layer on said two vertical sides;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides; and

said step of forming said gate electrode forms said gate electrode on said two vertical sides.

4. (original) A method according to claim 2, in which said step of patterning said epitaxial layer comprises forming an island having two vertical sides;

said step of forming said channel layer forms said channel layer on said two vertical sides;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides; and

said step of forming said gate electrode forms said gate electrode on said two vertical sides separated by a transverse distance.

5. (original) A method according to claim 1, in which said step of patterning said epitaxial layer comprises forming an island having two vertical sides separated by a transverse distance;

said step of forming said channel layer forms said channel layer on said two vertical sides and on a top surface of said island, whereby said channel layer on said top surface has said device lattice constant along said transverse distance and along said channel direction;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides and on said top surface; and

said step of forming said gate electrode forms said gate electrode on said two vertical sides and said top surface.

6. (original) A method according to claim 2, in which said step of patterning said epitaxial layer comprises forming an island having two vertical sides separated by a transverse distance;

said step of forming said channel layer forms said channel layer on said two vertical sides and on a top surface of said island, whereby said channel layer on said top surface has said device lattice constant along said transverse distance and along said channel direction;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides and on said top surface; and

said step of forming said gate electrode forms said gate electrode on said two vertical sides and said top surface.

7. (original) A method according to claim 1, further comprising a step of implanting said body area of said channel layer p-type, whereby said MOS transistor is an nfet.

8. (original) A method according to claim 1, further comprising a step of implanting said body area of said channel layer n-type, whereby said MOS transistor is a pfet.

9. (currently amended) A method of forming a MOS transistor comprising the steps of:

providing a semiconductor wafer of ~~a first semiconductor material~~ silicon having a device layer with a device layer lattice constant;

forming an epitaxial layer of a second semiconductor material on said device layer of said semiconductor wafer, said second material having a second lattice constant greater than said device lattice constant in a direction perpendicular to said wafer and said device layer lattice constant in a channel direction parallel to said wafer;

forming a fin hardmask in a transistor area of said wafer;

patterning said epitaxial layer of said second material to form a fin of said second semiconductor material having at least one vertical side in said channel direction between source and drain areas;

growing an epitaxial semiconductor channel layer of ~~said first semiconductor material~~ silicon on said vertical side, said channel layer having said second lattice constant perpendicular to said wafer and said device lattice constant along said channel direction, whereby said channel layer has tensile strain perpendicular to said channel direction and to said wafer;

forming a gate insulator in a body area of at least one vertical side of said channel layer;

forming a gate electrode abutting said gate insulator; and

forming source and drain electrodes in said source and drain areas and in contact with opposite ends of said body area.

10. (currently amended) A method according to claim 9, in which ~~said first semiconductor material is silicon and~~ said second semiconductor material is SiGe.

11. (original) A method according to claim 9, in which said step of patterning said epitaxial layer comprises forming a fin having two vertical sides separated by a transverse distance;

said step of forming said channel layer forms said channel layer on said two vertical sides;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides; and

said step of forming said gate electrode forms said gate electrode on said .two vertical sides.

12. (original) A method according to claim 10, in which said step of patterning said epitaxial layer comprises forming a fin having two vertical sides;

said step of forming said channel layer forms said channel layer on said two vertical sides;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides; and

said step of forming said gate electrode forms said gate electrode on said .two vertical sides separated by a transverse distance.

13. (original) A method according to claim 9, in which said step of patterning said epitaxial layer comprises forming a fin having two vertical sides separated by a transverse distance;

said step of forming said channel layer forms said channel layer on said two vertical sides and on a top surface of said fin, whereby said channel layer on said top surface has said device lattice constant along said transverse distance and along said channel direction;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides and on said top surface; and

said step of forming said gate electrode forms said gate electrode on said two vertical sides and said top surface.

14. (original) A method according to claim 10, in which said step of patterning said epitaxial layer comprises forming a fin having two vertical sides separated by a transverse distance;

said step of forming said channel layer forms said channel layer on said two vertical sides and on a top surface of said fin, whereby said channel layer on said top surface has said device lattice constant along said transverse distance and along said channel direction;

said step of forming said gate insulator forms said gate insulator on body areas of both said vertical sides and on said top surface; and

said step of forming said gate electrode forms said gate electrode on said two vertical sides and said top surface.

15. (original) A method according to claim 9, further comprising a step of implanting said body area of said channel layer p-type, whereby said MOS transistor is an nfet.

16. (original) A method according to claim 9, further comprising a step of implanting said body area of said channel layer n-type, whereby said MOS transistor is a pfet.

17. (withdrawn) An integrated circuit comprising a set of field effect transistors formed in a semiconductor wafer of a first semiconductor material having a device layer with a device layer lattice constant; and

an epitaxial layer of a second semiconductor material on said device layer of said semiconductor wafer, said second material having a second lattice constant greater than said device lattice constant in a direction perpendicular to said wafer and said device layer lattice constant in a channel direction parallel to said wafer; in which

said field effect transistors have an epitaxial semiconductor channel layer of said first semiconductor material on at least one vertical side of said epitaxial layer of said second semiconductor material, said channel layer having said second lattice constant perpendicular to said wafer and said device lattice constant along said channel direction, whereby said channel layer has tensile strain perpendicular to said channel direction and to said wafer;

said field effect transistors have a gate insulator in a body area of at least one vertical side of said channel layer;

said field effect transistors have a gate electrode abutting said gate insulator; and

said field effect transistors have source and drain electrodes in contact with opposite ends of said body area.

18. (withdrawn) An integrated circuit according to claim 17, in which said epitaxial layer is formed in a set of islands having two vertical sides separated by a transverse distance;

said epitaxial semiconductor channel layer of said first semiconductor material extends on two vertical sides and on a top surface of an island of said second semiconductor material, whereby said channel layer on said top surface has said

device lattice constant along said transverse distance and along said channel direction;

said gate insulator is formed on body areas of both said vertical sides and on said top surface; and

said gate electrode is formed on said gate electrode on said two vertical sides and said top surface.

19. (withdrawn) An integrated circuit according to claim 17, in which

said field effect transistors have two epitaxial semiconductor channel layers of said first semiconductor material on two sides of said fin of said second semiconductor material, said channel layers having said second lattice constant perpendicular to said wafer and said device lattice constant along said channel direction, whereby said channel layers have tensile strain perpendicular to said channel direction and to said wafer;

said field effect transistors have a gate insulator in a body area of said two channel layers;

said field effect transistors have a gate electrode abutting said gate insulator; and

said field effect transistors have source and drain electrodes in contact with opposite ends of said body area.

20. (withdrawn) An integrated circuit according to claim 19, in which:

said epitaxial semiconductor channel layer of said first semiconductor material extends on two vertical sides and on a top surface of said fin of said second

semiconductor material, whereby said channel layer on said top surface has said device lattice constant along said transverse distance and along said channel direction;

said gate insulator is formed on body areas of both said vertical sides and on said top surface; and

said gate electrode is formed on said gate electrode on said two vertical sides and said top surface.